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EXAMINER

KOSTAK, VICTOR R

ART UNIT	PAPER NUMBER
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2614

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/555,188
Filing Date: September 13, 2000
Appellant(s): STAHL ET AL.

Joseph S. Tripoli
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 07/22/04.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. The amendment after final rejection filed on 07/21/04 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bril (of record).

The receiver of Bril (noting particularly Figs. 1, 5A and 5B and the similarity with appellant's Fig. 3) involves a television system 100 that could be digital (e.g. col. 5 lines 28-31). The claimed means for receiving from a peripheral device reads on the input port of element 140 that accepts data on line 174. The claimed digital bus interconnection reads on bus 178 that interconnects OSD controller (which provides the bit-mapped on-screen display data: col. 6 lines 11-16) with the claimed means for receiving data from a peripheral device 110 (interface 110 ultimately connected to a source device not shown), by way of intermediate memory 180. Decoder 130 meets the claimed receiving means for receiving a digital stream representative of a video program (as it passes the television signals from element 120, which can be digital, as noted earlier). Multiplexer 140 meets the claimed means for combining as it accepts the digital video signal through line 134 and the bit-mapped OSD data through line 174, in turn generating a composite single stream to display unit 150, which ultimately displays a combined image (e.g. Fig. 5B), thereby meeting claim 1.

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As for claims 2 and 10, memory 180 receives subsequent bit maps from data provided at later times from network (again, originating from interface 110), and the combined display then shows an updated composite presentation (e.g. col. 10 line 13; col. 12 lines 15-23).

As for claim 3, the system of Bril can arrange the composite display in any of various presentation formats, including updating or removing of overlays, as would be expected (note, for example, col. 12 lines 14-23; col. 16 lines 11-18).

Regarding claim 4, multiple peripheral devices can be accessed, which would be on a selective basis (e.g. col. 5 lines 57-60; col. 7 lines 42-43).

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bril.

As for claim 7, the message indicative of characteristics of bit-mapped blocks reads on the position and size of the OSD overlay data (noting Figs. 5A and 5B, and further col. 9 lines 35-56 describing pointer data).

Furthermore regarding the asynchronous request to the peripheral device (through network interface 110), Bril neither specifies nor excludes allowability of any particular accessing mode. He does, however, provide flexibility in accessing individual OSD units from memory (col. 8 lines 40-48), which suggests to one of ordinary skill in the art that it would have been obvious to access upon request OSD data in an asynchronous mode, for the explicit purpose of providing access to data at any time not contingent on other functions.

As for claim 8, the message data includes both position and size data of the OSD data unit in question, as noted previously.

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Regarding claim 9, although Bril does not describe the OSD data in any form as a transport stream, it does pass through bus 178 and ultimately to display screen 150 in decoded form as a data stream. Since the data must be identified by various parameters including memory location, screen size and position data (noted above), as well as by intensity and color values, in order to be reproduced as viewable information (the data explicitly described in bit-map form elsewhere). It would therefore have been obvious to one of ordinary skill in the art to provide header-type data to correspond to the description data, with the appended bitstream qualifying as payload data.

(10) Response to Argument

The gist of appellant's argument is in two parts, is the same for both grounds of rejection, and is repeated in separate arguments for the three independent claims 1, 7 and 10.

The first part of his argument is that because the OSD controller 170 of Bril converts non-bit-mapped data types from memory 180 obtained from the peripheral device into bit-mapped form, then Bril therefore does not disclose receiving bit-mapped data from the peripheral device.

However (and as pointed out in the advisory action), a careful reading and reasonable interpretation of the claim does not require one of ordinary skill in the art to exclusively conclude that the peripheral device must directly and specifically generate bit-mapped data. Such is not explicit in the claim. Bril does indeed receive from a peripheral device bit-mapped data

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representative of OSD data by virtue of an intermediate processor (i.e. OSD controller 170) which formats the data into bit-mapped form.

The second part of appellant's argument is merely an extension of the first part. Maintaining the position that Bril does not generate bit-mapped data from the peripheral device, appellant argues that Bril therefore does not disclose combining the bit-mapped data received from the peripheral device with the digital stream to produce a combined displayable image.

The examiner counters by pointing out that the data from the peripheral device is in bit-mapped form (again, because of controller stage 170), and therefore the bit-mapped data and the digital stream (of video data) are in fact combined by element 140 for subsequent display as a combined image.

Appellant does not argue the rationale of the obviousness rejection applied against claims 7-9, but instead, as noted above, relies on the view that Bril does not provide bit-mapped data originating from the peripheral device.

The dependent claims are not argued separately but are also presumed allowable by appellant by virtue of their dependency.

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Respectfully submitted,

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Primary Examiner
Art Unit 2614



VRK
December 16, 2004

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